Objectives:

**Lab01 Vivado**

* Logic
  + WS <-> TT <-> CD <-> Verilog
* Verilog
  + Working with the Vivado IDE
  + Creating a module in Verilog
  + Logical operators
  + Concurrent Signal Assignments
* Simulation
  + Working with testbenches
  + Working with ModelSim (run command)
  + Creating timing diagrams
  + Verifying design
* Synthesis

**Lab02 Hex to 7-segment**

* Logic
  + TT <-> Verilog
* Verilog
  + Always statement
  + Vectors (forming and breaking apart)
* Simulation
  + Adding color to traces
* Synthesis
  + Pin assignment to module signals

**Lab03 Rock Paper Scissors**

* Logic
  + Module-level design
* Verilog
  + Creating and instantiating modules
* Simulation
* Synthesis

**Lab04 High/Low Guessing Game**

* Logic
  + BBB
* Verilog
  + Generics
  + LFSR
  + Using basic building blocks
    - 3:8 decoder
    - 2:1 mux
    - Compare
    - Mux
    - Hex2Seven
* Simulation
  + Use of Do files
* Synthesis

**Lab05 High/Low Guessing Game with hints**

* Logic
* Verilog
  + Using basic building blocks
    - Adder Subtractor
* Simulation
* Synthesis

**Lab06 Basic Calculator**

* Logic
  + 2’s complement
  + Arithmetic
* Verilog
* Simulation
* Synthesis

**Lab07 Cellular Automata**

* Logic
  + Simple FSM
  + Cellular automata
* Verilog
  + D flip flop
* Simulation
* Synthesis

Lab08 Clock Divider Not Implemented

**Lab09 mod10Counter**

* Logic
* Verilog
  + Circuits with state
* Simulation
* Synthesis

**Lab10 Stopwatch Datapath**

* Logic
  + Datapath
* Verilog
* Simulation
* Synthesis

**Lab 11 Stopwatch Control**

* Logic
  + FSM
* Verilog
* Simulation
* Synthesis

**Lab 12 Stopwatch**

* Logic
  + Datapath and Control
* Verilog
* Simulation
* Synthesis